Transceiver Signal Integrity Development Kit

Stratix V GX Edition User Guide

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Additional Information

The Altera® Stratix® V GX Transceiver Signal Integrity Development Kit is a complete design environment that includes both the hardware and software you need to develop Stratix V GX FPGA designs. The one-year license for the Quartus® II software provides everything you need to begin developing custom Stratix V GX FPGA designs. The following list describes what you can accomplish with the kit:

■ Evaluate transceiver performance from 600 Mbps up to 12.5 Gbps.

■ Generate and check pseudo-random binary sequence (PRBS) patterns.

■ Dynamically change differential output voltage (V_{OD}) pre-emphasis, and equalization settings to optimize transceiver performance for your channel.

■ Perform jitter analysis.

■ Verify physical medium attachment (PMA) compliance to PCI Express®(PCIe®), Gbps Ethernet (GbE), XAUI, CEI-6G, Serial RapidIO®, high-definition serial digital interface (HD-SDI), and other major standards.

Kit Features

This section briefly describes the Transceiver Signal Integrity Development Kit, Stratix V GX Edition contents.

Hardware

The Transceiver Signal Integrity Development Kit, Stratix V GX Edition includes the following hardware:

■ Stratix V GX transceiver signal integrity development board—A development platform that allows you to develop and prototype hardware designs running on the Stratix V GX FPGA.

    For detailed information about the board components and interfaces, refer to the *Transceiver Signal Integrity Development Kit Stratix V GX Reference Manual*.

■ Power supply and cables—The kit includes the following items:

    ■ Power supply and AC adapters for North America/Japan, Europe, and the United Kingdom

    ■ USB type A to B cable

    ■ Ethernet cable

Software

The software for this kit, described in the following sections, is available on the Altera website for immediate downloading. You can also request to have Altera mail the software to you on DVDs.

Quartus II Software

Your kit includes a license for the Development Kit Edition (DKE) of the Quartus II software (Windows platform only). For one year, this license entitles you to most of the features of the Subscription Edition (excluding the IP Base Suite).

☞ After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software. For more information, refer to the Design Software page of the Altera website.

The Quartus II Development Kit Edition (DKE) software includes the following items:

- Quartus II Software—The Quartus II software, including the Qsys system integration tool, provides a comprehensive environment for network on a chip (NoC) design. The Quartus II software integrates into nearly any design environment and provides interfaces to industry-standard EDA tools.

- MegaCore® IP Library—A library that contains Altera IP MegaCore functions. You can evaluate MegaCore functions by using the OpenCore Plus feature to do the following:

  - Simulate behavior of a MegaCore function within your system.

  - Verify functionality of your design, and quickly and easily evaluate its size and speed.

  - Generate time-limited device programming files for designs that include MegaCore functions.

  - Program a device and verify your design in hardware.

  ☞ The OpenCore Plus hardware evaluation feature is an evaluation tool for prototyping only. You must purchase a license to use a MegaCore function in production.

  👣 For more information about OpenCore Plus, refer to *AN 320: OpenCore Plus Evaluation of Megafunctions*.

- Nios® II Embedded Design Suite (EDS)—A full-featured set of tools that allows you to develop embedded software for the Nios II processor which you can include in your Altera FPGA designs.

Development Kit Installer

The license-free Transceiver Signal Integrity Development Kit, Stratix V GX Edition, installer includes all the documentation and design examples for the kit.

☞ For information on the development kit installer, refer to "Installing the Development Kit" on page 3–3.

The remaining chapters in this user guide lead you through the following development board setup steps:

- Inspecting the contents of the kit

- Installing the design and kit software

- Setting up, powering up, and verifying correct operation of the transceiver signal integrity development board

- Configuring the Stratix V GX FPGA

- Running the Board Test System designs

For complete information about this development board, refer to the *Transceiver Signal Integrity Development Kit Stratix V GX Reference Manual*.

Before You Begin

Before using the kit or installing the software, check the kit contents and inspect the board to verify that you received all of the items listed in "Kit Features" on page 1–1. If any of the items are missing, contact Altera before you proceed.

Inspect the Board

To inspect the board, perform the following steps:

1. Place the board on an anti-static surface and inspect it to ensure that it has not been damaged during shipment.

    ⚠ CAUTION   Without proper anti-static handling, you can damage the board.

2. Verify that all components are on the board and appear intact.

3. For proper Stratix V GX device cooling, install the heatsink/fan included with the kit using the provided heatsink/fan installation tool.

For more information about power consumption and thermal modeling, refer to *AN 358: Thermal Management for FPGAs*.

References

Use the following links to check the Altera website for other related information:

- For the latest board design files and reference designs, refer to the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page.

- For the Stratix V GX device documentation, refer to the Literature: Stratix V Devices page.

- To purchase devices from the eStore, refer to the Devices page.

■ For Stratix V GX OrCAD symbols, refer to the Capture CIS Symbols page.

■ For Nios II 32-bit embedded processor solutions, refer to the Embedded Processing page.

This chapter explains how to install the following software:

■ Quartus II Subscription Edition Software

■ Transceiver Signal Integrity Development Kit, Stratix V GX Edition

■ USB-Blaster™ driver

Installing the Quartus II Subscription Edition Software

The Quartus II Subscription Edition Software provides the necessary tools used for developing hardware and software for Altera devices. Included in the Quartus II Subscription Edition Software are the Quartus II software, the Nios II EDS, and the MegaCore IP Library. The Quartus II software (including Qsys) and the Nios II EDS are the primary FPGA development tools used to create the reference designs in this kit. To install the Altera development tools, perform the following steps:

1. Download the Quartus II Subscription Edition Software from the Quartus II Subscription Edition Software page of the Altera website. Alternatively, you can request a DVD from the Altera IP and Software DVD Request Form page of the Altera website.

2. Follow the on-screen instructions to complete the installation process.

    If you have difficulty installing the Quartus II software, refer to *Altera Software Installation and Licensing Manual*.

Licensing Considerations

Purchasing this kit entitles you to a one-year license for the Development Kit Edition (DKE) of the Quartus II software.

☞ After the year, your DKE license will no longer be valid and you will not be permitted to use this version of the Quartus II software. To continue using the Quartus II software, you should download the free Quartus II Web edition or purchase a subscription to Quartus II software.

Before using the Quartus II software, you must activate your license, identify specific users and computers, and obtain and install a license file.

If you already have a licensed version of the subscription edition, you can use that license file with this kit. If not, you need to obtain and install a license file. To begin, go to the Self Service Licensing Center page of the Altera website, log into or create your myAltera account, and take the following actions:

1. On the Activate Products page, enter the serial number provided with your development kit in the **License Activation Code** box.

☞ Your serial number is printed on the development kit box below the bottom bar code. The number is 10 or 11 alphanumeric characters and does not contain hyphens. Figure 3–1 shows *3S150SPXXXX* as an example serial number.

Figure 3–1. Locating Your Serial Number

2. Consult the Activate Products table, to determine how to proceed.

   a. If the administrator listed for your product is someone other than you, skip the remaining steps and contact your administrator to become a licensed user.

   b. If the administrator listed for your product is you, proceed to step 3.

   c. If the administrator listed for your product is *Stocking*, activate the product, making you the administrator, and proceed to step 3.

3. Use the Create New License page to license your product for a specific user (you) on specific computers. The Manage Computers and Manage Users pages allow you to add users and computers not already present in the licensing system.

   ☞ To license the Quartus II software, you need your computer's network interface card (NIC) ID, a number that uniquely identifies your computer. On the computer you use to run the Quartus II software, type `ipconfig /all` at a command prompt to determine the NIC ID. Your NIC ID is the 12-digit hexadecimal number on the **Physical Address** line.

4. When licensing is complete, Altera emails a **license.dat** file to you. Store the file on your computer and use the **License Setup** page of the **Options** dialog box in the Quartus_II software to enable the software.

👣 For complete licensing details, refer to *Altera Software Installation and Licensing Manual*.

Installing the Development Kit

To install the Transceiver Signal Integrity Development Kit, Stratix V GX Edition, perform the following steps:

1. Download the kit installer from the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page of the Altera website. Alternatively, you can request a development kit DVD from the Altera Kit Installations DVD Request Form page of the Altera website.

2. Run the Transceiver Signal Integrity Development Kit, Stratix V GX Edition, installer.

3. Follow the on-screen instructions to complete the installation process.

> **CAUTION** Be sure that the installation directory you choose is in the same relative location to the Quartus II software installation.

The installation program creates the development kit directory structure shown in Figure 3–2.

Figure 3–2. Installed Development Kit Directory Structure [1]

<install dir>
The default Windows installation directory is **C:\altera**<version>\.
    kits
        stratixVGX_5sgxea7nf40_si
            board_design_files
            demos
            documents
            examples
            factory_recovery
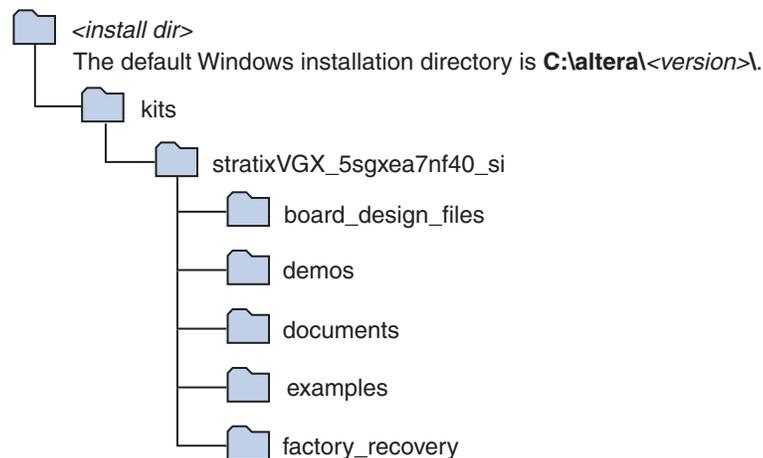
Note to Figure 3–2:

(1) Early-release versions might have slightly different directory names.

Table 3–1 lists the file directory names and a description of their contents.

Table 3–1. Installed Directory Contents

Directory Name	Description of Contents
board_design_files	Contains schematic, layout, assembly, and bill of material board design files. Use these files as a starting point for a new prototype board design.
demos	Contains demonstration applications when available.
documents	Contains the development kit documentation.
examples	Contains the sample design files for the development kit.
factory_recovery	Contains the original data programmed onto the board before shipment. Use this data to restore the board with its original factory contents.

Installing the USB-Blaster Driver

The Stratix V GX transceiver signal integrity development board includes integrated USB-Blaster circuitry for FPGA programming. However, for the host computer and board to communicate, you must install the USB-Blaster driver on the host computer.

Installation instructions for the USB-Blaster driver for your operating system are available on the Altera website. On the Altera Programming Cable Driver Information page of the Altera website, locate the table entry for your configuration and click the link to access the instructions.

The instructions in this chapter explain how to set up the Stratix V GX transceiver signal integrity development board.

Setting Up the Board

To prepare and apply power to the board, perform the following steps:

1. The Stratix V GX transceiver signal integrity development board ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be currently configured with the default settings, follow the instructions in "Factory Default Switch Settings" on page 4–2 to return the board to its factory settings before proceeding.

2. The transceiver signal integrity development board ships with design examples stored in the flash memory device. Verify the Load Selector (J28) is set to the jump pins 2-3 position to load the design stored in the factory portion of flash memory. Figure 4–1 shows the switch location on the Stratix V GX transceiver signal integrity development board. Connect the 120 W, 20 VDC @ 6.32 A power supply (model # LTE120E-SW-3XX) to the DC Power Jack (J1) on the FPGA board and plug the cord into a power outlet.

    ⚠ **CAUTION** Use only the supplied power supply. Power regulation circuitry on the board can be damaged by power supplies with greater voltage.

3. Set the POWER switch (SW1) to the on position. When power is supplied to the board, Power blue LED (D3) illuminates indicating that the board has power.

The MAX II device on the board contains (among other things) a parallel flash loader (PFL) megafunction. When the board powers up, the PFL reads a design from flash memory and configures the FPGA. The Load Selector (J28) controls which design to load: When in the jump pins 2-3 position, the PFL loads the design from the factory portion of flash memory. When in the jump pins 1-2 position, the PFL loads the design from the user portion of flash memory.

☞ The kit includes a MAX II design which contains the MAX II PFL megafunction. The design resides in the *<install dir>***kits\stratixVGX_5sgxea7nf40_si\examples\max2** directory.

When configuration is complete, one of two LEDs illuminate, (D10 for `FACTORY_IMAGE` or D11 for `USER_IMAGE`) signaling that the Stratix V GX device configured successfully. If either configuration fails, the `CONFIG_ERR` LED (D9) illuminates.

👣 For more information about the PFL megafunction, refer to *AN 386: Parallel Flash Loader Megafunction User Guide*.

Factory Default Switch Settings

This section shows the factory switch settings for the Stratix V GX transceiver signal integrity development board.

Figure 4–1 shows the switch locations and the default position of each switch on the top side of the board.

Figure 4–1. Switch Locations and Default Settings on the Board Top
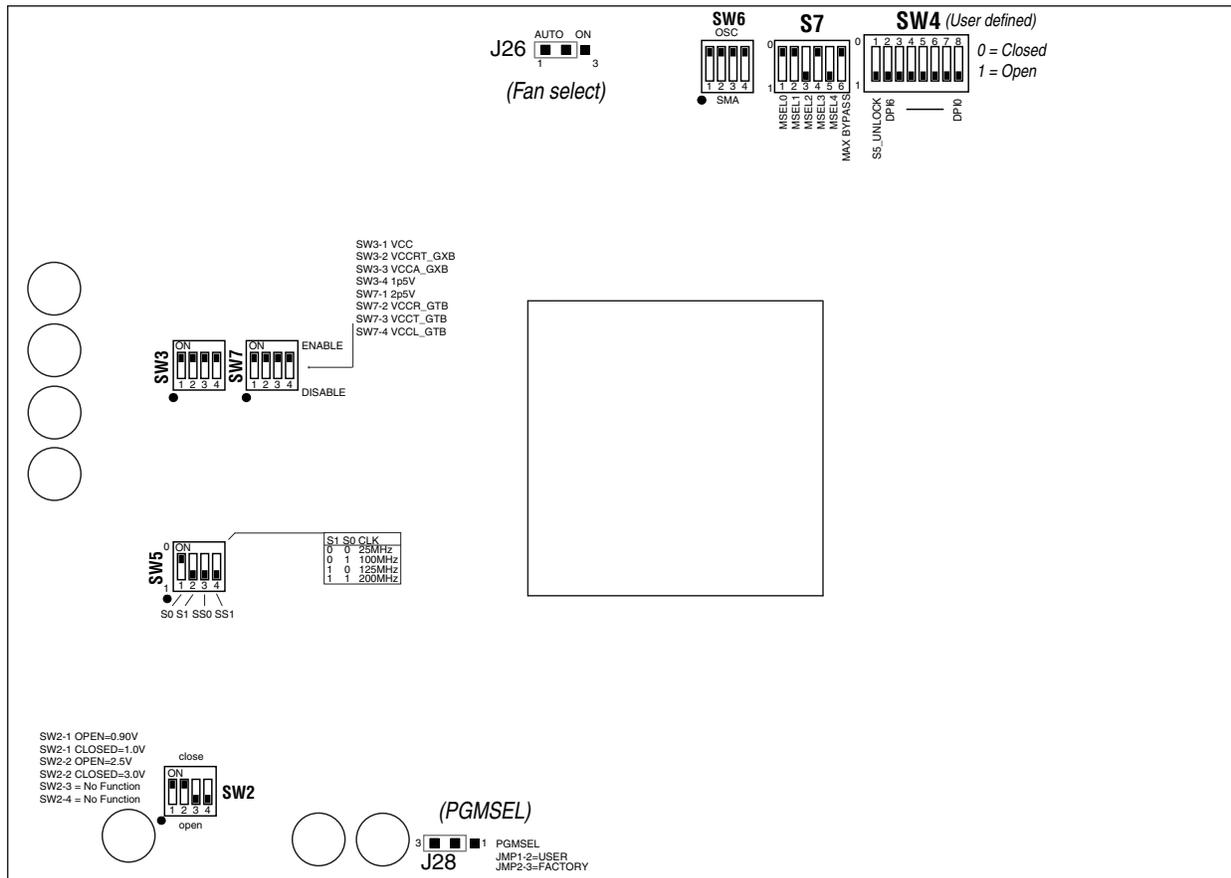
To restore the switches to their factory default settings, perform the following steps:

1. Set the DIP switch bank (SW2) to match Table 4–1 and Figure 4–1.

Table 4–1. SW2 Dip Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	SW2-1 [(1)]	Switch 1 has the following options: ■ Open = VCCRT_GXB select at 0.90 V ■ Close = VCCRT_GXB select at 1.0 V	Close
2	SW2-2 [(1)]	Switch 2 has the following options: ■ Open = VCCA_GXB select at 2.5 V ■ Close = VCCA_GXB select at 3.0 V	Close

Table 4–1. SW2 Dip Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	SW2-3	Switch 3 has the following options: ■ Open = No function ■ Closed = No function	—
4	SW2-4	Switch 4 has the following options: ■ Open = No function ■ Closed = No function	—

Note to: Table 4–1

(1) If the board is powered off and powered on again with SW2-1 and -2 in the open position, the voltage rails VCCRT_GXB and VCCA_GXB will not come up to their proper levels. To ensure that the voltage rails VCCRT_GXB and VCCA_GXB come up to their proper levels, set SW2-1 and -2 to the default closed position at power up. Once the board has power, change the rail voltages as you prefer.

2. For power sequencing, set DIP switch bank (SW3) to match Table 4–2 and Figure 4–1. (For the other power sequence settings, see Table 4–6.)

Table 4–2. SW3 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	SW3-1 VCC	Switch 1 has the following power sequencing options: ■ S5GX_VCC is enabled. ■ S5GX_VCC is disabled.	ENABLED
2	SW3-2 VCCRT_GXB	Switch 2 has the following power sequencing options: ■ VCCRT_GXB is enabled. ■ VCCRT_GXB is disabled.	ENABLED
3	SW3-3 VCCA_GXB	Switch 3 has the following power sequencing options: ■ VCCA_GXB is enabled. ■ VCCA_GXB is disabled.	ENABLED
4	SW3-4 1p5V	Switch 4 has the following power sequencing options: ■ 1p5V is enabled. ■ 1p5V is disabled.	ENABLED

3. Set DIP switch bank (SW4) to match Table 4–3 and Figure 4–1.

Table 4–3. SW4 User Dip Switch Settings

Switch	Board Label	Function	Default Position
1	S5_UNLOCK	Switch 1 has the following options: ■ Closed = FACTORY command won't be issued. JTAG will be locked out if FPGA is configured on power-up from flash. ■ Open = Unlock the FPGA and allow FACTORY command. JTAG will be available even if FPGA is configured on power-up from flash.	Open
2–8	DPI6—DPI0	User defined options.	—

4. Set DIP switch bank (SW5) to match Table 4–4 and Figure 4–1.

Table 4–4. SW5 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	S0	Determines S5GX_CKL11 frequency. [1]	1
2	S1	Determines S5GX_CKL11 frequency.	0
3	SS0	Determines S5GX_CKL11 spectrum spread. [1]	0
4	SS1	Determines S5GX_CKL11 spectrum spread.	0

Note to: Table 4–4

(1) Truth tables for the SW5 settings:
S1 S0 Frequency
00 25 MHz
01 100 MHz (default)
10 125 MHz
11 200 MHz
SS1 SS0 Spread%
00 center =/- 25%
01 down -0.5%
10 down -0.75%
11 no spread (default)

5. Set DIP switch bank (SW6) to match Table 4–5 and Figure 4–1.

Table 4–5. SW6 Dip Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	REFCLK_SEL_U32	Switch 1 has the following options: ■ When set at OSC, enables oscillator input. ■ When set at SMA, enables SMA input.	OSC
2	REFCLK_SEL_U33	Switch 2 has the following options: ■ When set at OSC, enables oscillator input. ■ When set at SMA, enables SMA input.	OSC

Table 4–5. SW6 Dip Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	REFCLK_SEL_U34	Switch 3 has the following options: ■ When set at OSC, enables oscillator input. ■ When set at SMA, enables SMA input.	OSC
4	REFCLK_SEL_U35	Switch 4 has the following options: ■ When set at OSC, enables oscillator input. ■ When set at SMA, enables SMA input.	OSC

6. For power sequencing, set DIP switch bank (SW7) to match Table 4–6 and Figure 4–1. (For the other power sequence settings, see Table 4–2.)

Table 4–6. SW7 Dip Switch Settings

Switch	Board Label	Function	Default Position
1	SW7-1 2p5V	Switch 1 has the following power sequencing options: ■ 2p5V is enabled. ■ 2p5V is disabled.	ENABLED
2	SW7-2 VCCR_GTB	Switch 2 has the following power sequencing options: ■ VCCR_GTB is enabled. ■ VCCR_GTB is disabled.	ENABLED
3	SW7-3 VCCT_GTB	Switch 3 has the following power sequencing options: ■ VCCT_GTB is enabled. ■ VCCT_GTB is disabled.	ENABLED
4	SW7-4 VCCL_GTB	Switch 4 has the following power sequencing options: ■ VCCL_GTB is enabled. ■ VCCL_GTB is disabled.	ENABLED

7. Set DIP switch bank (S7) to match Table 4–7 and Figure 4–1.

Table 4–7. S7 Dip Switch Settings (Part 1 of 2)

Switch	Board Label	Function	Default Position
1	MSEL0	Switch 1 has the following options: ■ Logic 0. ■ Logic 1.	0
2	MSEL1	Switch 2 has the following options: ■ Logic 0. ■ Logic 1.	0

Table 4–7. S7 Dip Switch Settings (Part 2 of 2)

Switch	Board Label	Function	Default Position
3	MSEL2	Switch 3 has the following options: ■ Logic 0. ■ Logic 1.	1
4	MSEL3	Switch 4 has the following options: ■ Logic 0. ■ Logic 1.	0
5	MSEL4	Switch 5 has the following options: ■ Logic 0. ■ Logic 1.	1
6	MAX BYPASS	Switch 6 has the following options: ■ Logic 0. Includes the MAX II device in the JTAG chain. ■ Logic 1. Removes the MAX II device in the JTAG chain.	0

8. Set jumper blocks (J26, J28) to match Table 4–8 and Figure 4–1.

Table 4–8. Jumper Settings

Board Reference	Description	Shunt Position
J26	Fan select — Pins 1-2 select auto operation.	Installed
J26	Fan select — Pins 2-3 select fan on.	Not installed
J28	PGMSEL (logic 1) — Pins 1-2 select user-defined image.	Not Installed
J28	PGMSEL (logic 0) — Pins 2-3 select factory image.	Installed

☞ For more information about the FPGA board settings, refer to the *Transceiver Signal Integrity Development Kit Stratix V GX Reference Manual*.

The Transceiver Signal Integrity Development Kit, Stratix V GX Edition, ships with the Board Update Portal design example stored in the factory portion of the flash memory on the board. The design consists of a Nios II embedded processor, an Ethernet MAC, and an HTML web server.

When you power up the board with the Load Selector (J28) in the factory position (jump pins 2-3), the Stratix V GX FPGA configures with the Board Update Portal design example. The design can obtain an IP address from any DHCP server and serve a web page from the flash on your board to any host computer on the same network. The web page allows you to upload new FPGA designs to the user portion of flash memory, and provides links to useful information on the Altera website, including kit-specific links and design resources.

☞ After successfully updating the user flash memory, you can load the user design from flash memory into the FPGA. To do so, set the Load Selector (J28) to the user position (jump pins 1-2) and power cycle the board.

The source code for the Board Update Portal design resides in the *<install dir>***kits\stratixVGX_5sgxea7nf40_si\examples** directory. If the Board Update Portal is corrupted or deleted from the flash memory, refer to "Restoring the Flash Device to the Factory Settings" on page A–4 to restore the board with its original factory contents.

Connecting to the Board Update Portal Web Page

This section provides instructions to connect to the Board Update Portal web page.

☞ Before you proceed, ensure that you have the following:

■ A PC with a connection to a working Ethernet port on a DHCP enabled network.

■ A separate working Ethernet port connected to the same network for the board.

■ The Ethernet and power cables that are included in the kit.

To connect to the Board Update Portal web page, perform these steps:

1. With the board powered down, set the Load Selector (J28) to the factory position (jump pins 2-3).

2. Attach the Ethernet cable from the board to your LAN.

3. Power up the board. The board connects to the LAN's gateway router, and obtains an IP address. The LCD on the board displays the IP address.

4. Launch a web browser on a PC that is connected to the same network, and enter the IP address from the LCD into the browser address bar. The Board Update Portal web page appears in the browser.

☞ You can click **Transceiver Signal Integrity Development Kit, Stratix V GX Edition** on the Board Update Portal web page to access the kit's home page for documentation updates and additional new designs.

👣 You can also navigate directly to the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page of the Altera website to determine if you have the latest kit software.

Using the Board Update Portal to Update User Designs

The Board Update Portal allows you to write new designs to the user portion of flash memory. Designs must be in the Nios II Flash Programmer File (**.flash**) format.

☞ Design files available from the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page include **.flash** files. You can also create **.flash** files from your own custom design. Refer to "Preparing Design Files for Flash Programming" on page A–2 for information about preparing your own design for upload.

To upload a design over the network into the user portion of flash memory on your board, perform the following steps:

1. Perform the steps in "Connecting to the Board Update Portal Web Page" to access the Board Update Portal web page.

2. In the **Hardware File Name** field specify the **.flash** file that you either downloaded from the Altera website or created on your own. If there is a software component to the design, specify it in the same manner using the **Software File Name** field; otherwise, leave the **Software File Name** field blank.

3. Click **Upload**. The progress bar indicates the percent complete. The file takes about 20 seconds to upload.

4. To configure the FPGA with the new design after the flash memory upload process is complete, set the Load Selector (J28) to the user position (jump pins 1-2), and power cycle the board.

☞ As long as you don't overwrite the factory image in the flash memory device, you can continue to use the Board Update Portal to write new designs to the user portion of flash memory. If you do overwrite the factory image, you can restore it by following the instructions in "Restoring the Flash Device to the Factory Settings" on page A–4.

The kit includes a design example and an application called the Board Test System to test the functionality of the Stratix V GX transceiver signal integrity development board. The application provides an easy-to-use interface to alter functional settings and observe the results. You can use the application to test board components, modify functional parameters, observe performance, and measure power usage. (While using the application, you reconfigure the FPGA several times with test designs specific to the functionality you are testing.) The application is also useful as a reference for designing systems. To install the application, follow the steps in "Installing the Development Kit" on page 3–3.

The Board Test System communicates over the JTAG bus to a test design running in the Stratix V GX device. Figure 6–1 shows the initial GUI for a board that is in the factory configuration.

Figure 6–1. Board Test System Graphical User Interface
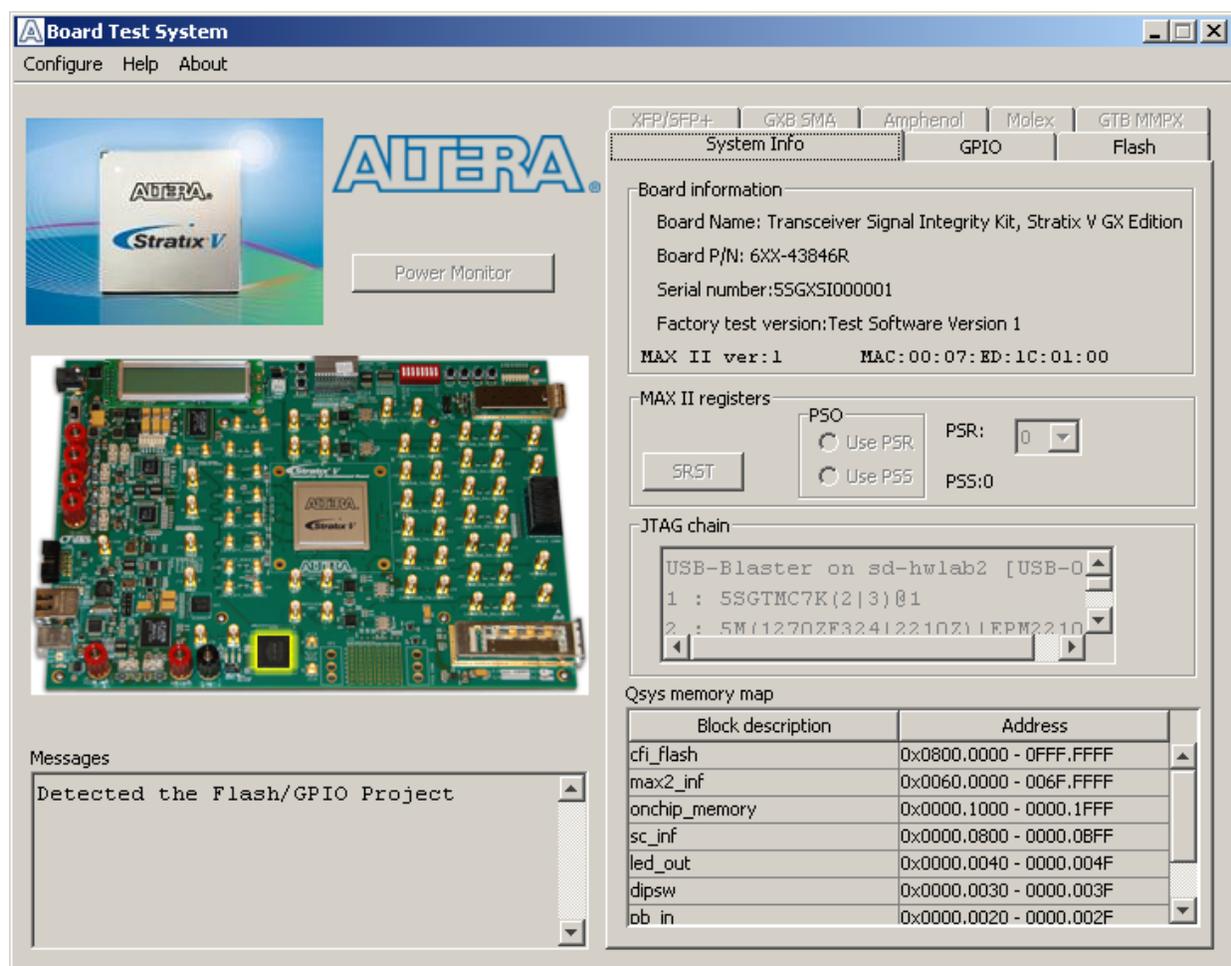
Several designs are provided to test the major board features. Each design provides data for one or more tabs in the application. The Configure menu identifies the appropriate design to download to the FPGA for each tab.

After successful FPGA configuration, the appropriate tab appears and allows you to exercise the related board features. Highlights appear in the board picture around the corresponding components.

☞ The Board Test System and Power Monitor share the JTAG bus with other applications like the Nios II debugger and the SignalTap® II Embedded Logic Analyzer. Because the Quartus II programmer uses most of the bandwidth of the JTAG bus, other applications using the JTAG bus might time out. Be sure to close the other applications before attempting to reconfigure the FPGA using the Quartus II Programmer.

Preparing the Board

With the power to the board off, following these steps:

1. Connect the USB cable to the board.

    ☞ If you connect an external USB-Blaster download cable and power cycle the board, the on-board Blaster is disconnected and the S5_UNLOCK function (Table 4–3 on page 4–4) does not allow JTAG access to the FPGA. To successfully use the USB-Blaster cable, disconnect it before power cycling the board. After you power cycled the board, then reconnect the USB-Blaster cable.

2. Ensure that the development board DIP switches are set to the default positions as shown in the "Factory Default Switch Settings" section starting on page 4–2.

3. Install a jumper at the user position (jump pins 1-2) of the Load Selector (J28) jumper block.

    👣 For more information about the board's DIP switch and jumper settings, refer to the *Transceiver Signal Integrity Development Kit Stratix V GX Reference Manual*.

4. Turn on the power to the board. The board loads the design stored in the user portion of flash memory into the FPGA. If your board is still in the factory configuration, or if you have downloaded a newer version of the Board Test System to flash memory through the Board Update Portal, the design loads the GPIO,SRAM, and flash memory tests.

    ⚠ CAUTION To ensure operating stability, keep the USB cable connected and the board powered on when running the demonstration application. The application cannot run correctly unless the USB cable is attached and the board is on.

Running the Board Test System

To run the application, navigate to the
<*install dir*>**kits\stratixVGX_5sgxea7nf40_si\examples\board_test_system**
directory and run the **BoardTestSystem.exe** application.

☞ In Windows, click **Start** > **All Programs** > **Altera** > **Transceiver Signal Integrity Development Kit, Stratix V GX Edition** <*version*> > **Board Test System** to run the application.

A GUI appears, displaying the application tab that corresponds to the design running in the FPGA. The Stratix V GX transceiver signal integrity development board's flash memory ships preconfigured with the design that corresponds to the GPIO and Flash tabs.

☞ If you power up your board with the Load Selector (J28) in the factory position (jump pins 2-3), or if you load your own design into the FPGA with the Quartus II Programmer, you receive a message prompting you to configure your board with a valid Board Test System design. Refer to "The Configure Menu" for information about configuring your board.

Using the Board Test System

This section describes each control in the Board Test System application.

The Configure Menu

Use the Configure menu (Figure 6–2) to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 6–2. The Configure Menu
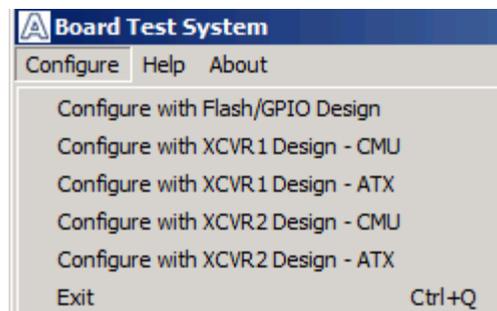
To configure the FPGA with a test system design, perform the following steps:

1. On the Configure menu, click the configure command that corresponds to the functionality you wish to test.

2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (**.sof**) to the FPGA. The download process usually takes less than a minute.

> **⚠ CAUTION** Ensure that the version of Quartus II software set in the `$QUARTUS_ROOTDIR` environment variable matches the version of files you have installed (not required for service packs). For example, the Development Kit Installer version 11.1.2 requires that the Quartus II software version 11.0 or 11.1 to be installed. You can set this variable by starting the required 32-bit Quartus II software version.

3. When configuration finishes, close the Quartus II Programmer, if open. The design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled.

The System Info Tab

The **System Info** tab shows information about the board's current configuration. Figure 6–1 on page 6–1 shows the **System Info** tab. The tab displays the contents of the MAX II registers, the JTAG chain, the board's MAC address, the flash memory map, and other details stored on the board.

The following sections describe the controls on the **System Info** tab.

Board Information

The **Board information** control displays static information about your board.

■ **Board Name**—Indicates the official name of the board, given by the Board Test System.

■ **Board P/N**—Indicates the part number of the board.

■ **Serial number**—Indicates the serial number of the board.

■ **Factory test version**—Indicates the version of the Board Test System used to production test the board.

■ **MAX II ver**—Indicates the version of MAX II code currently running on the board. The MAX II code resides in the *<install dir>***\kits\stratixVGX_5sgxea7nf40_si\examples** directory. Newer revisions of this code might be available on the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page of the Altera website.

■ **MAC**—Indicates the MAC address of the board.

MAX II Registers

The **MAX II registers** control allows you to view and change the current MAX II register values as described in Table 6–1. Changes to the register values with the GUI take effect immediately.

Table 6–1. MAX II Registers

Register Name	Read/Write Capability	Description
System Reset (SRST)	Write only	Set to 0 to initiate an FPGA reconfiguration.
Page Select Override (PSO)	Read / Write	When set to 0, the value in PSR determines the page of flash memory to use for FPGA reconfiguration. When set to 1, the value in PSS determines the page of flash memory to use for FPGA reconfiguration.
Page Select Switch (PSS)	Read only	Holds the current value of jumper J28 PGMSEL: 1 = user image 2 = factory image.
Page Select Register (PSR)	Read / Write	Determines which of the up to eight (0-7) pages of flash memory to use for FPGA reconfiguration. The flash memory ships with pages 0 and 1 preconfigured.

- **SRST**—Resets the system and reloads the FPGA with a design from flash memory based on the other MAX II register values. Refer to Table 6–1 for more information.

- **PSO**—Sets the MAX II PSO register. The following options are available:

    - **Use PSR**—Allows the PSR to determine the page of flash memory to use for FPGA reconfiguration.

    - **Use PSS**—Allows the PSS to determine the page of flash memory to use for FPGA reconfiguration.

- **PSR**—Sets the MAX II PSR register. The numerical values in the list corresponds to the page of flash memory to load during FPGA reconfiguration. Refer to Table 6–1 for more information.

- **PSS**—Displays the MAX II PSS register value. Refer to Table 6–1 for the list of available options.

☞ Because the **System Info** tab requires that a specific design is running in the FPGA at a specific clock speed, writing a 0 to SRST or changing the PSO value can cause the Board Test System to stop running.

JTAG Chain

The **JTAG chain** control shows all the devices currently in the JTAG chain. The Stratix V GX device is always the first device in the chain.

☞ When set to 0, switch S7.6 (MAX BYPASS) includes the MAX II device in the JTAG chain; when set to 1, the MAX II device is removed from the JTAG chain.

Qsys Memory Map

The **Qsys memory map** control shows the memory map of the flash memory device on your board.

The GPIO Tab

The **GPIO** tab allows you to interact with all the general purpose user I/O components on your board. You can write to the character LCD, read DIP switch settings, turn LEDs on or off, and detect push button presses. Figure 6–3 shows the **GPIO** tab.

Figure 6–3. The GPIO Tab
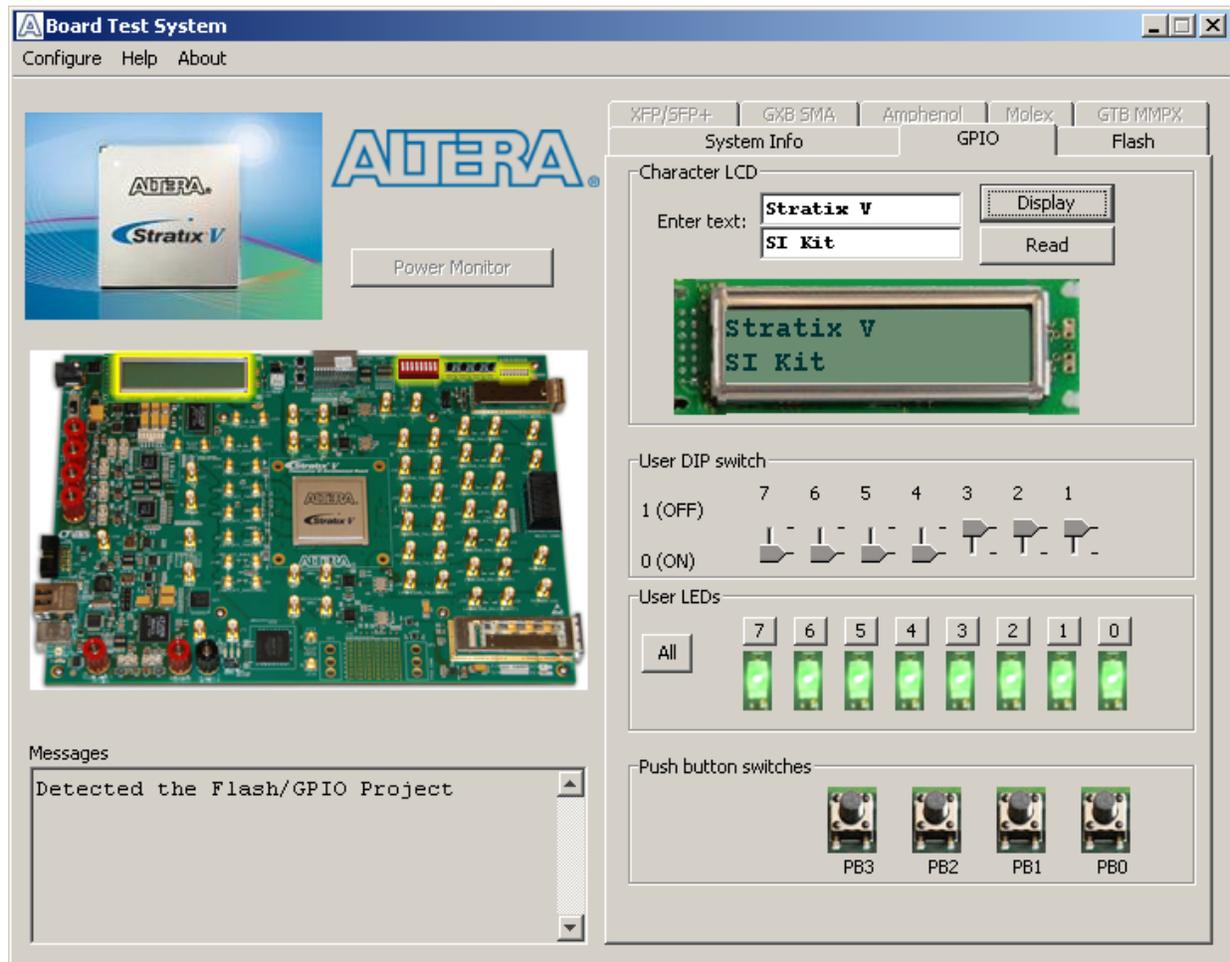
The following sections describe the controls on the **GPIO** tab.

Character LCD

The **Character LCD** controls allow you to display text strings on the character LCD on your board. Type text in the text boxes and then click **Display**.

☞ If you exceed the 16 character display limit on either line, a warning message appears.

User DIP Switches

The read-only **User DIP switches** control displays the current positions of the switches in the user DIP switch bank (SW4). Change the switches on the board to see the graphical display change accordingly.

User LEDs

The **User LEDs** control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off.

Push Button Switches

The read-only **Push button switches** control displays the current state of the board user push buttons. Press a push button on the board to see the graphical display change accordingly.

The Flash Tab

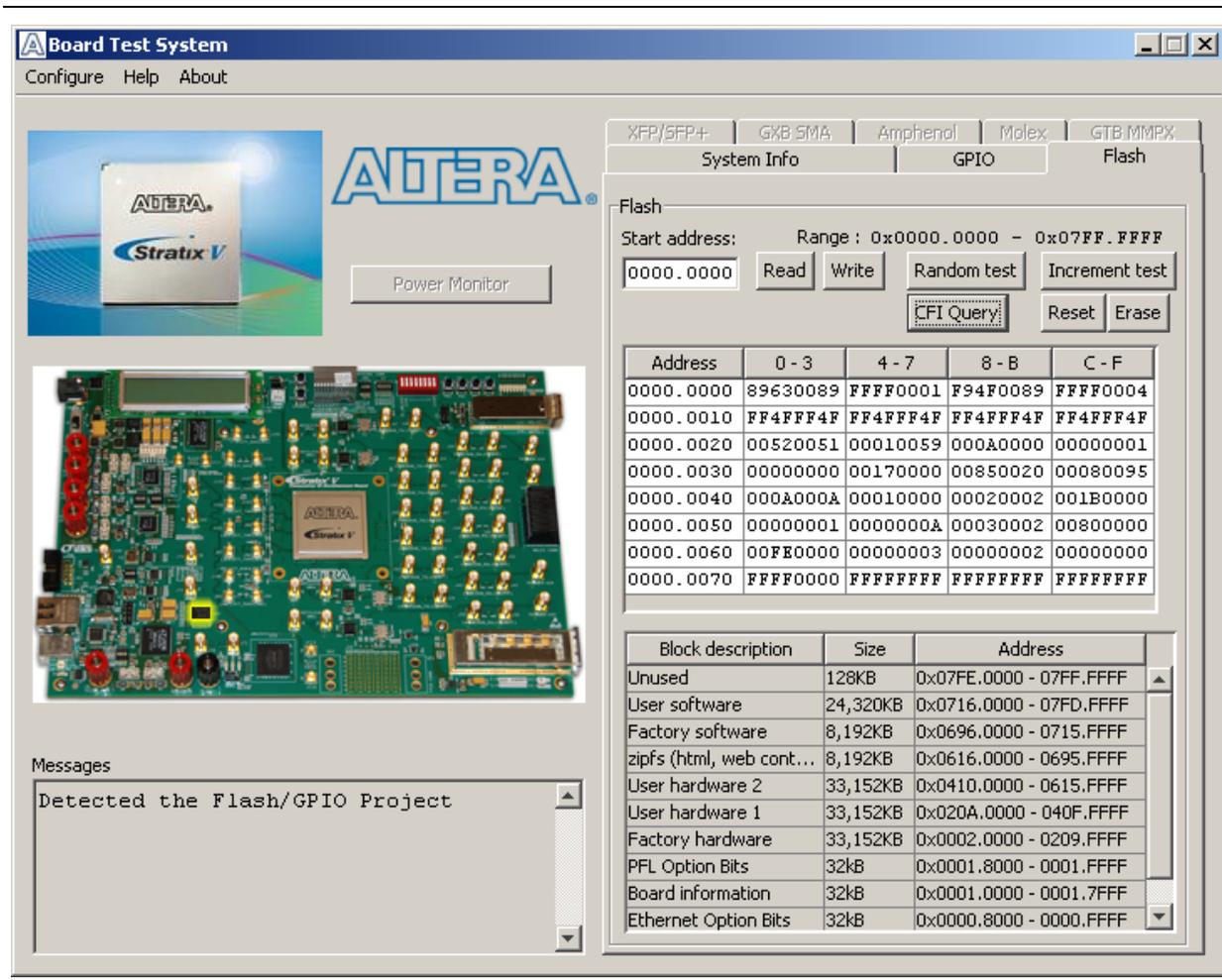The **Flash** tab allows you to read and write flash memory on your board. Figure 6–4 shows the **Flash** tab.

Figure 6–4. The Flash Tab

The following sections describe the controls on the **Flash** tab.

Read

The **Read** control reads the flash memory on your board. To see the flash memory contents, type a starting address in the text box and click **Read**. Values starting at the specified address appear in the table. The flash memory sits at a base address of 0x0800.0000. To see flash memory contents type the address above the base and values starting at this address are displayed. Valid entries are 0x0000.0000 through 0x07FF.FFFF.

☞ If you enter an address outside of 0x0000.0000 to 0x07FF.FFFF flash memory address space, a warning message identifies the valid flash memory address range.

Write

The **Write** control writes the flash memory on your board. To update the flash memory contents, change values in the table and click **Write**. The application writes the new values to flash memory and then reads the values back to guarantee that the graphical display accurately reflects the memory contents.

☞ To prevent overwriting the dedicated portions of flash memory, the application limits the writable flash memory address range to 0x08FE.0000 to 0x08FF.FFFF (which corresponds to address range 0x0000.0000 - 0x003FF.FFF in the uppermost portion of the user software memory block, as shown in Figure 6–1 on page 6–1 and Table A–1 on page A–1).

Random Test

Starts a random data pattern test to flash memory, which is limited to a scratch page in the upper 128K block.

CFI Query

The **CFI Query** control updates the memory table, displaying the CFI ROM table contents from the flash device.

Increment Test

Starts an incrementing data pattern test to flash memory, which is limited to scratch page in the upper 128K block.

Reset

The **Reset** control executes the flash device's reset command and updates the memory table displayed on the **Flash** tab.

Erase

Erases flash memory, which is limited to a scratch page in the upper 128K block.

Flash Memory Map

Displays the flash memory map for the Transceiver Signal Integrity Development Kit.

The GXB SMA Tab

The **GXB SMA** tab allows you to run transceiver SMA loopback tests on your board. You can also load the design and use an oscilloscope to measure an eye diagram of the SMA transmit signals. Figure 6–5 shows the **GXB SMA** tab.

Figure 6–5. The GXB SMA Tab
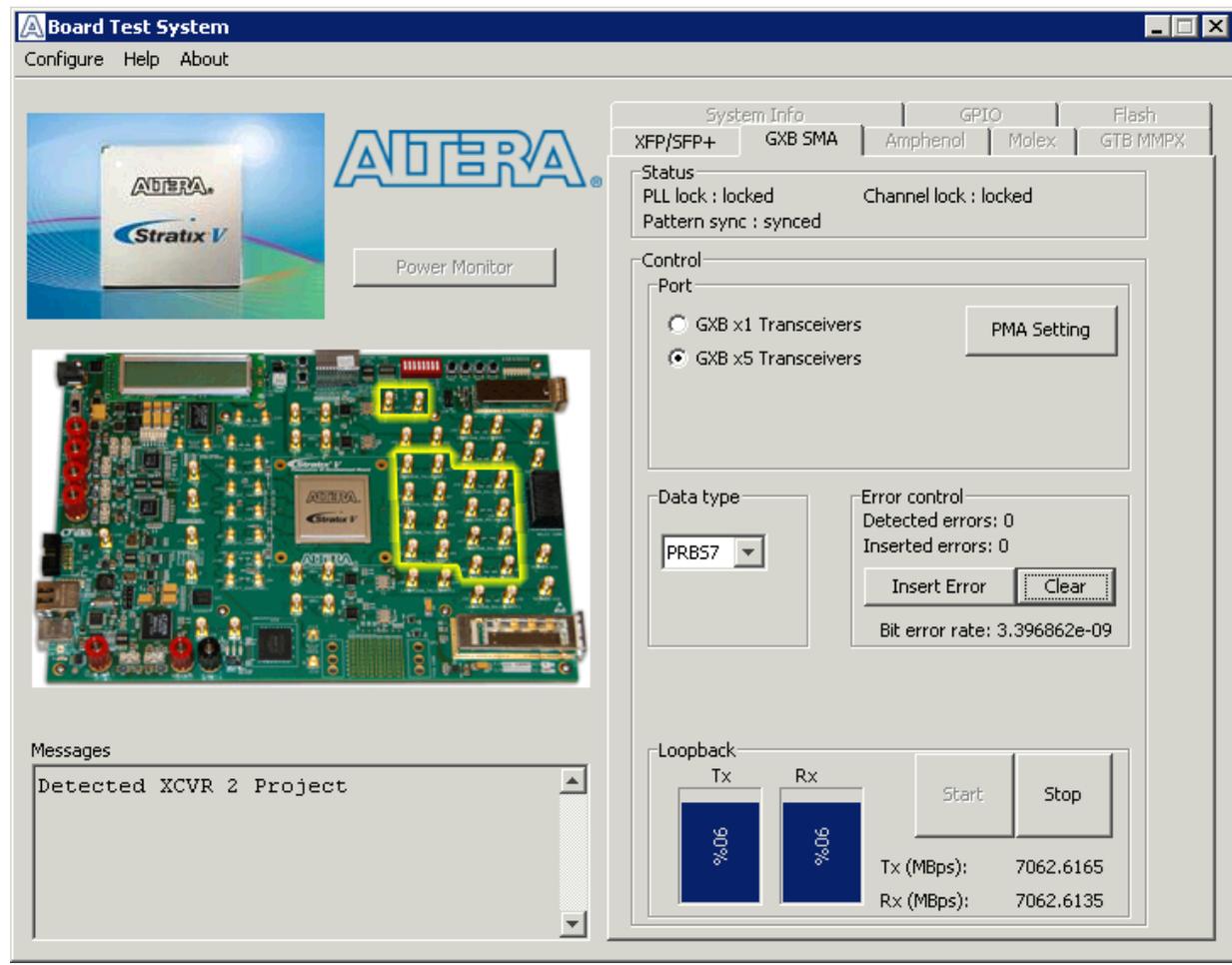
The following sections describe the controls on the **GXB SMA** tab.

Status

The **Status** control displays the following status information during the loopback test:

■ **PLL lock**—Shows the PLL locked or unlocked state.

■ **Channel lock**—Shows the channel locked or unlocked state for multi-channel designs only. When locked, all lanes are word aligned and channel bonded.

■ **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port

■ **GXB x1 Transceivers**—Controls the following single transceiver channel:
{GXB_RXLp_11}
{GXB_TXLp_11}

■ **GXB x5 Transceivers**—Controls controls the following five transceiver channels:
{GXB_RXLp_17, GXB_RXLp_15, GXB_RXLp_14, GXB_RXLp_13, GXB_RXLp_12}
{GXB_TXLp_17, GXB_TXLp_15, GXB_TXLp_14, GXB_TXLp_13, GXB_TXLp_12}

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

■ **Serial Loopback**—Routes signals between the transmitter and the receiver. Enter the following values to enable the serial loopbacks:

0 = high speed serial transceiver signals to loopback on the board
1 = serial loopback (TX to RX)
2 = reverse serial loopback pre-CDR (RX to TX)
4 = reverse serial loopback post-CDR (RX to TX)

☞ On Altera devices, serial loopback multiplexes data from the TX high speed serial buffer to the RX high speed serial buffer. Reverse serial loopback multiplexes data from the RX high speed serial buffer to the TX high speed serial buffer.

■ **VOD**—Specifies the voltage output differential of the transmitter buffer.

■ **Pre-emphasis tap**

■ **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.

■ **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.

■ **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.

■ **Equalizer**—Specifies the setting for the receiver equalizer.

■ **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. Select the following available data types for analysis:

■ **PRBS7** —pseudo-random 7-bit sequences (default)

■ **PRBS15**—pseudo-random 15-bit sequences

■ **PRBS23**—pseudo-random 23-bit sequences

■ **PRBS31**—pseudo-random 31-bit sequences

■ **HF1**—highest frequency divide-by-2 data pattern "10101010"

■ **HF2**—next highest frequency divide-by-6 data pattern "111000111000"

■ **HF3**—second lowest frequency divide-by-22 data pattern

■ **LF** —lowest frequency divide by 33 data pattern

☞ Settings HF1, HF2, HF3, LF are for transmit observation only and are not intended for use in the receiver data detection circuitry.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

■ **Detected errors**—Displays the number of data errors detected in the received bit stream.

■ **Inserted errors**—Displays the number of errors inserted into the transmit data stream.

■ **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.

■ **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Loopback

■ **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

■ **Start**—This control initiates the loopback tests.

■ **Stop**—This control terminates the loopback tests.

■ **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

GTB MMPX Tab

The **GTB MMPX** tab is only available with the Stratix X GT device and is grayed out for this release.

The XFP/SFP+ Tab

The **XFP/SFP+** tab allows you to run an XFP or SPF optical loopback test. You can also run the test using an electrical loopback test if you do not have an SFP or XFP module with optical loopback fibre available. Figure 6–6 shows the **XFP/SFP+** tab.

☞ To test the board using an XFP optical module from the BTS, if the optical module requires a divide by 64 REFCLK, perform the following steps before powering on the board:

1. Set SW6[1] (8:1) to open (SMA), and SW6[2] (7:2) to closed.

2. Connect differential clock cables from SMAs J72/73 to J79/J80.

Figure 6–6. The XFP/SFP+ Tab
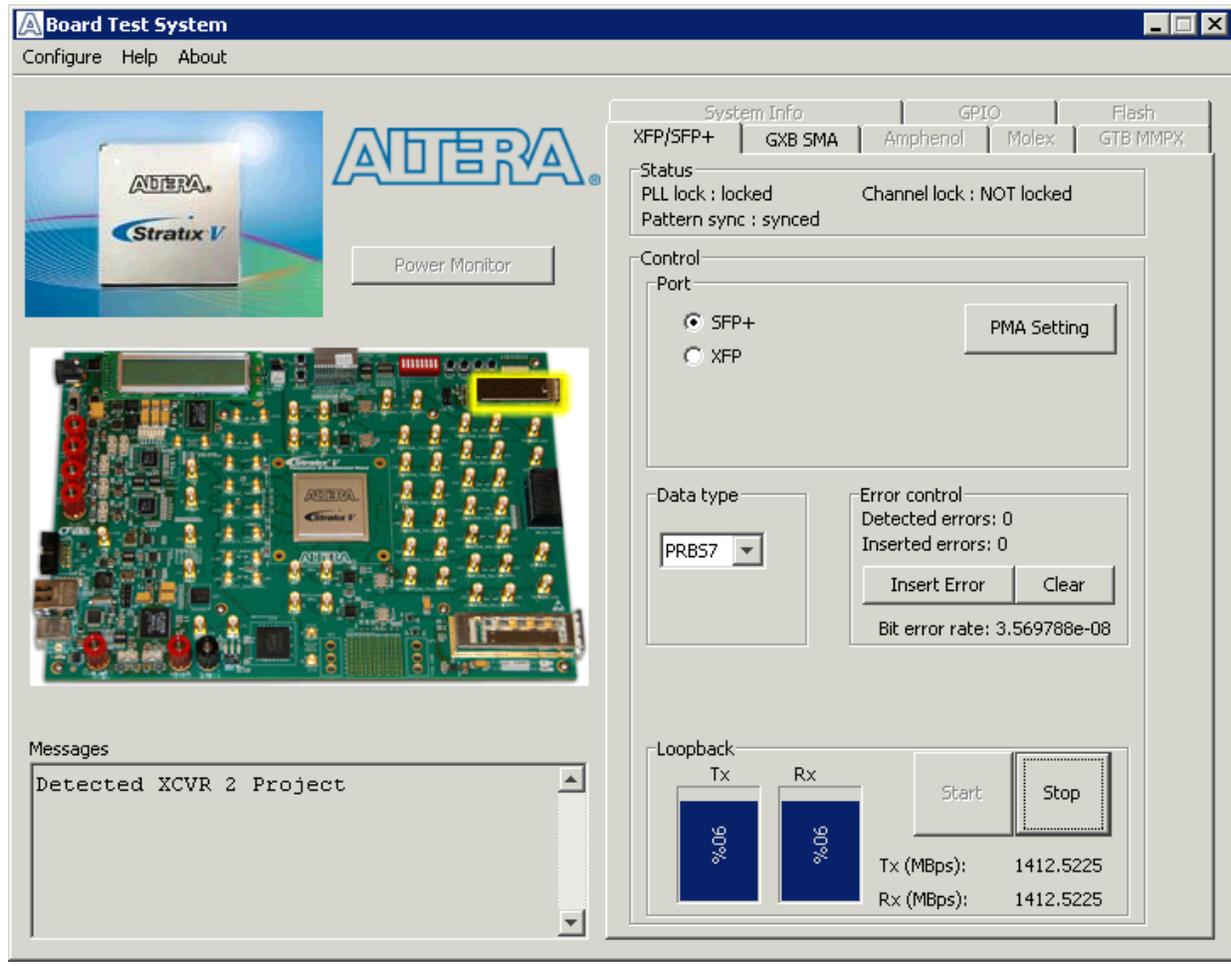
The following sections describe the controls on the **XFP/SFP+** tab.

Status

The **Status** control displays the following status information during the loopback test:

- **PLL lock**—Shows the PLL locked or unlocked state.

- **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded. Channel lock will always display *NOT locked* for single channel designs.

- **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port

Use the following controls to select an interface to apply PMA settings, data type and error control:

- SFP+

- XFP

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver to the transmitter.

- **VOD**—Specifies the voltage output differential of the transmitter buffer.

- **Pre-emphasis tap**

  - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.

  - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.

  - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.

- **Equalizer**—Specifies the setting for the receiver equalizer.

- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. Select the following available data types for analysis:

- **PRBS7** —pseudo-random 7-bit sequences (default)

- **PRBS15**—pseudo-random 15-bit sequences

- **PRBS23**—pseudo-random 23-bit sequences

- **PRBS31**—pseudo-random 31-bit sequences

- **HF1**—highest frequency divide-by-2 data pattern "10101010"

- **HF2**—next highest frequency divide-by-6 data pattern "111000111000"

- **HF3**—second lowest frequency divide-by-22 data pattern

- **LF** —lowest frequency divide by 33 data pattern

  ☞ Settings HF1, HF2, HF3, LF are for transmit observation only and are not used in the receiver data detection circuitry.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the received bit stream.

- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.

■ **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.

■ **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Loopback

■ **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

■ **Start**—This control initiates the loopback tests.

■ **Stop**—This control terminates the loopback tests.

■ **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

The Amphenol Tab

The **Amphenol** tab allows you to run a x4 backplane loopback test through the Amphenol connector. Figure 6–7 shows the **Amphenol** tab.

Figure 6–7. The Amphenol Tab
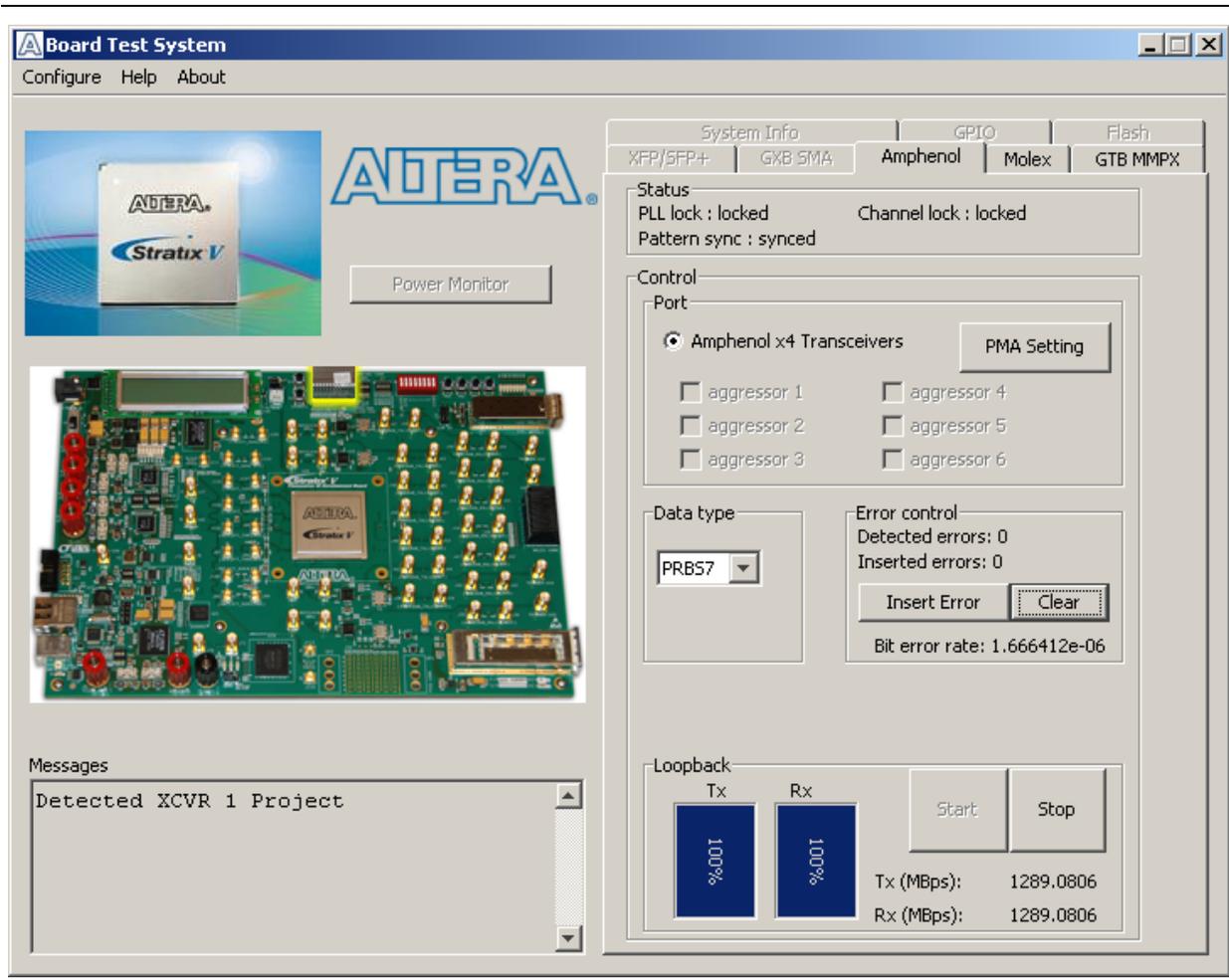
☞ No loopback is provided. A loopback backplane can be purchased from Amphenol.

The following sections describe the controls on the **Amphenol** tab.

Status

The **Status** control displays the following status information during the loopback test:

■ **PLL lock**—Shows the PLL locked or unlocked state.

■ **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.

■ **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port

The **Port** control allows you to specify the type of test to run on the Amphenol port. The following Amphenol port tests are available:

■ **Amphenol x4 Transceivers**

    ■ **aggressor 1 to 6**—If available, turning on an aggressor box will turn on the adjacent *aggressor* channels adding switching noise to the *victim* channel to be used for backplane analysis**.**

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

■ **Serial Loopback**—Routes signals between the receiver to the transmitter.

■ **VOD**—Specifies the voltage output differential of the transmitter buffer.

■ **Pre-emphasis tap**

    ■ **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.

    ■ **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.

    ■ **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.

■ **Equalizer**—Specifies the setting for the receiver equalizer.

■ **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. Select the following available data types for analysis:

■ **PRBS7** —pseudo-random 7-bit sequences (default)

■ **PRBS15**—pseudo-random 15-bit sequences

■ **PRBS23**—pseudo-random 23-bit sequences

- **PRBS31**—pseudo-random 31-bit sequences
- **HF1**—highest frequency divide-by-2 data pattern "10101010"
- **HF2**—next highest frequency divide-by-6 data pattern "111000111000"
- **HF3**—second lowest frequency divide-by-22 data pattern
- **LF** —lowest frequency divide by 33 data pattern

> ☞ Settings HF1, HF2, HF3, LF are for transmit observation only and are not used in the receiver data detection circuitry.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.
- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.
- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.
- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Loopback

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Start**—This control initiates the loopback tests.
- **Stop**—This control terminates the loopback tests.
- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

The Molex Tab

The **Molex** tab allows you to run an x4 backplane loopback test through the Molex connector. Figure 6–8 shows the **Molex** tab.

Figure 6–8. The Molex Tab
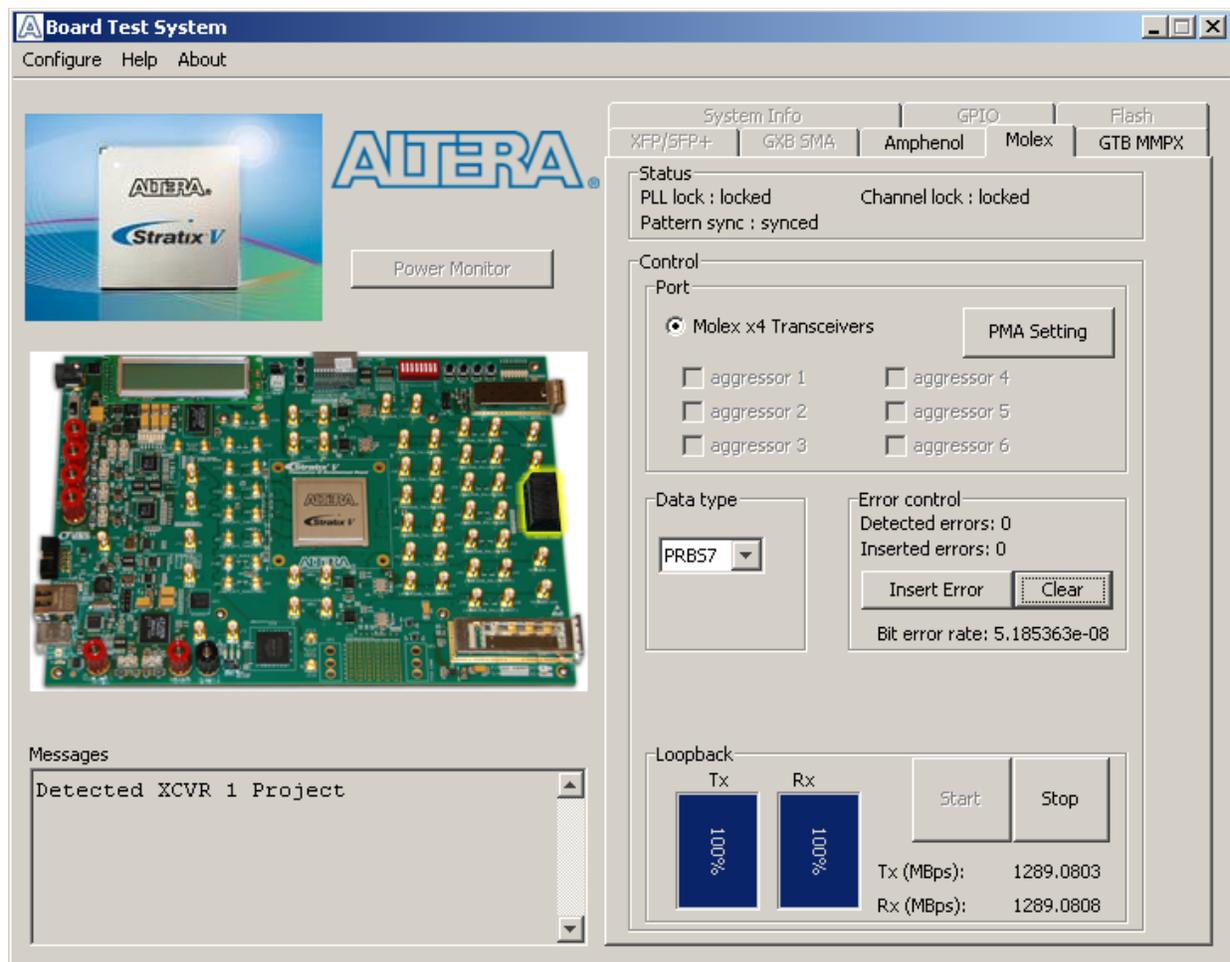
☞   No loopback board is provided. A loopback backplane can be purchased from Molex.

The following sections describe the controls on the **Molex** tab.

Status

The **Status** control displays the following status information during the loopback test:

■   **PLL lock**—Shows the PLL locked or unlocked state.

■   **Channel lock**—Shows the channel locked or unlocked state. When locked, all lanes are word aligned and channel bonded.

■   **Pattern sync**—Shows the pattern synced or not synced state. The pattern is considered synced when the start of the data sequence is detected.

Port

The **Port** control allows you to specify the type of test to run on the Molex port. The following Molex port tests are available:

- **Molex x1 Transceivers**

    - **aggressor 1 to 6**—If available, turning on an aggressor box will turn on the adjacent *aggressor* channels adding switching noise to the *victim* channel to be used for backplane analysis.

PMA Setting

The PMA Setting button allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback**—Routes signals between the receiver to the transmitter.

- **VOD**—Specifies the voltage output differential of the transmitter buffer.

- **Pre-emphasis tap**

    - **Pre**—Specifies the amount of pre-emphasis on the pre-tap of the transmitter buffer.

    - **First post**—Specifies the amount of pre-emphasis on the first post tap of the transmitter buffer.

    - **Second post**—Specifies the amount of pre-emphasis on the second post tap of the transmitter buffer.

- **Equalizer**—Specifies the setting for the receiver equalizer.

- **DC gain**—Specifies the DC portion of the receiver equalizer.

Data Type

The **Data type** control specifies the type of data contained in the transactions. Select the following available data types for analysis:

- **PRBS7** —pseudo-random 7-bit sequences (default)

- **PRBS15**—pseudo-random 15-bit sequences

- **PRBS23**—pseudo-random 23-bit sequences

- **PRBS31**—pseudo-random 31-bit sequences

- **HF1**—highest frequency divide-by-2 data pattern "10101010"

- **HF2**—next highest frequency divide-by-6 data pattern "111000111000"

- **HF3**—second lowest frequency divide-by-22 data pattern

- **LF** —lowest frequency divide by 33 data pattern

    ☞ Settings HF1, HF2, HF3, LF are for transmit observation only and are not used in the receiver data detection circuitry.

Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected errors**—Displays the number of data errors detected in the hardware.

- **Inserted errors**—Displays the number of errors inserted into the transmit data stream.

- **Insert Error**—Inserts a one-word error into the transmit data stream each time you click the button. **Insert Error** is only enabled during transaction performance analysis.

- **Clear**—Resets the **Detected errors** and **Inserted errors** counters to zeros.

Loopback

- **TX** and **RX** performance bars—Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.

- **Start**—This control initiates the loopback tests.

- **Stop**—This control terminates the loopback tests.

- **Tx (MBps)** and **Rx (MBps)**—Show the number of bytes of data analyzed per second.

Power Monitoring

To measure and view current power information for the transceiver signal integrity development board, you need install the free LTpowerPlay™ software, and then connect your PC and the development board to a Linear Technology DC1613A USB-to-PMBus Controller. Both the software and the controller interface are available from the Linear Technology (www.linear.com) website. Figure 6–9 shows the LTpowerPlay **GUI**.

Figure 6–9. LTpowerPlay
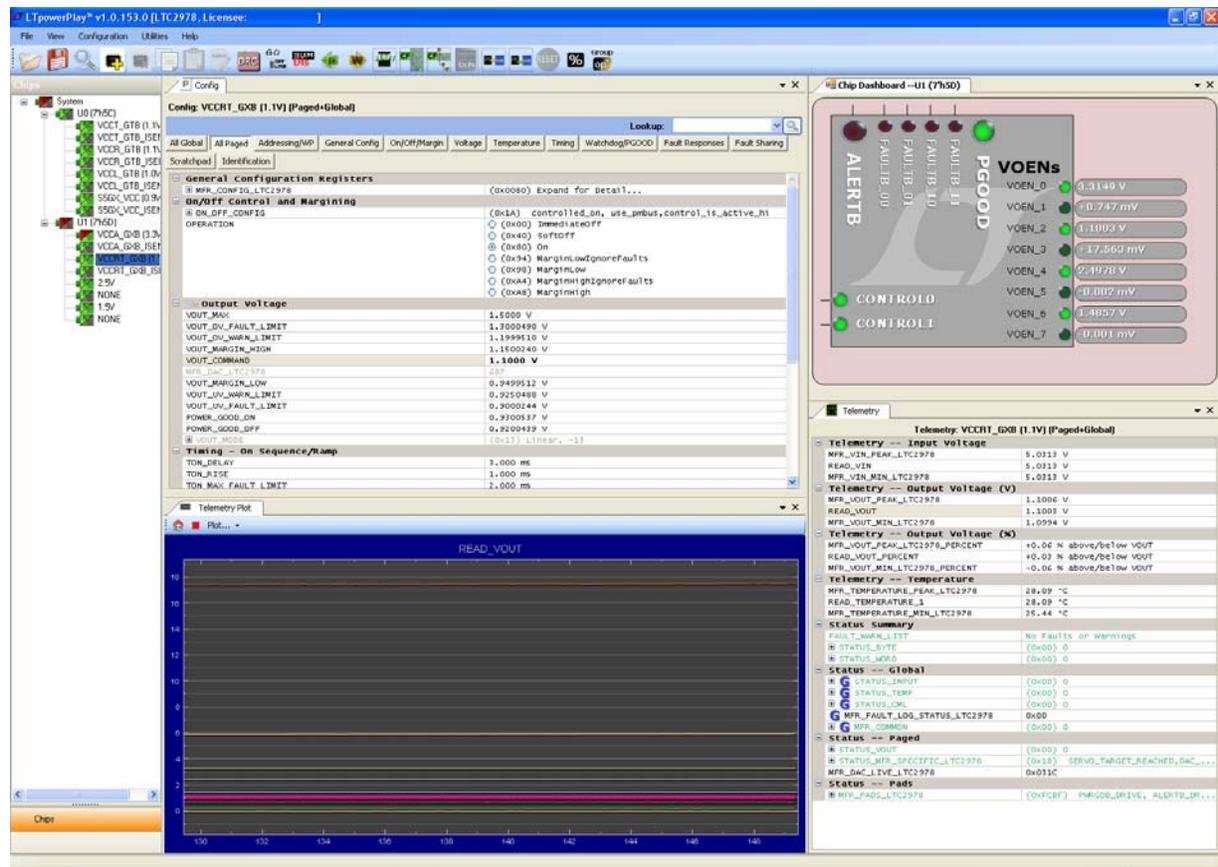
☞ The DC1613A USB-to-PMBus controller communicates with the LTC®2978 on-board octal PMBus power supply monitor and controller at the U10/11 board reference. For more information on the LTC2978, refer to the *Transceiver Signal Integrity Development Kit Stratix V GX Reference Manual.*

⚠ **CAUTION** The LTC 2978 power monitor devices installed on this board are programmed with a project file that sets up each voltage rail according to a sequence. Each voltage rail will adjust to its voltage level to within tolerance. However, if the development board is powered off and powered on again with SW2 in the open position, the voltage rails VCCRT_GXB and VCCA_GXB will not come up to the proper levels unless SW2-1 and SW2-2 are set to the default closed position at power up. For SW2 switch settings, refer to the default settings in Table 4–1 on page 4–2.

The Clock Control

The Clock Control application sets the Si570 programmable oscillator to any frequency between 10 MHz and 945 MHz and select frequencies to 1400 MHz. The oscillator drives a 2-to-4 buffer that drives a copy of the clock to all four edges of the FPGA.

The Clock Control application runs as a stand-alone application. **ClockControl.exe** resides in the
<*install dir*>**kits\\stratixVGX_5sgxea7nf40_si\\examples\\board_test_system** directory.

On Windows, click **Start** > **All Programs** > **Altera** > **Transceiver Signal Integrity Development Kit, Stratix V GX Edition** <*version*> > **Clock Control** to start the application.

For more information about the Si570 and the Stratix V GX transceiver signal integrity development board's clocking circuitry and clock input pins, refer to the *Transceiver Signal Integrity Development Kit Stratix V GX Reference Manual*.

The Clock Control communicates with the MAX II device on the board through the JTAG bus. The Si570 programmable oscillator is connected to the MAX II device through a 2-wire serial bus. Figure 6–10 shows the Clock Control.

Figure 6–10. The Clock Control
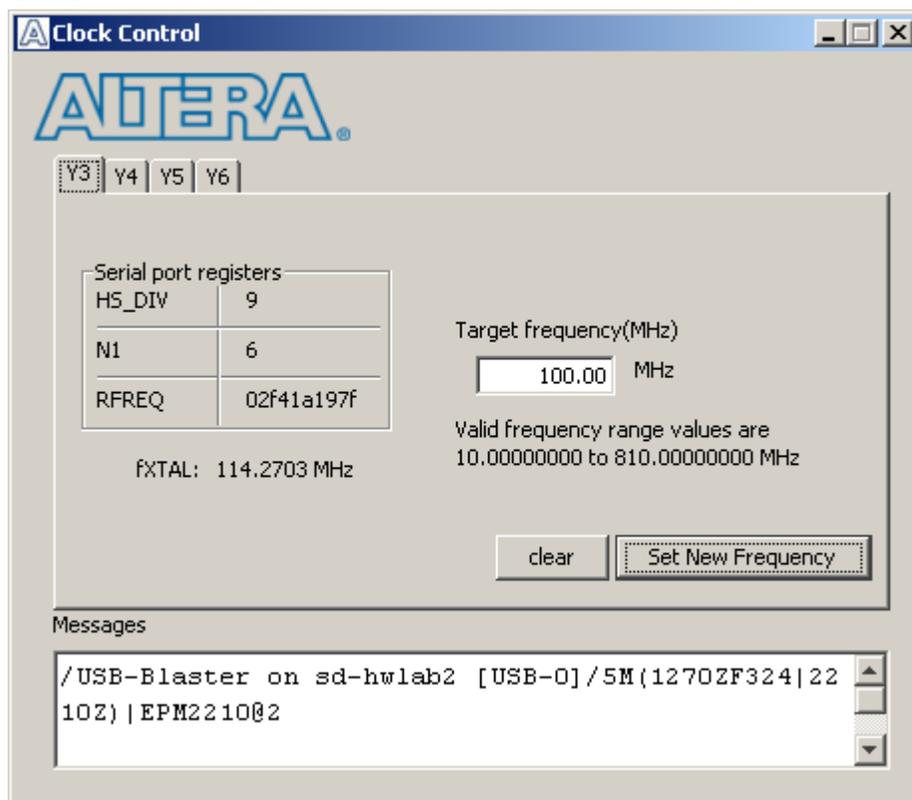
The following sections describe the Clock Control controls.

Serial Port Registers

The **Serial port registers** control shows the current values from the Si570 registers.

For more information about the Si570 registers, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

fXTAL

The **fXTAL** control shows the calculated internal fixed-frequency crystal, based on the serial port register values.

For more information about the f_{XTAL} value and how it is calculated, refer to the *Si570/Si571* data sheet available on the Silicon Labs website (www.silabs.com).

Target Frequency

The **Target frequency** control allows you to specify the frequency of the clock. Legal values are between 10 and 945 MHz and select frequencies to 1400 MHz. For example, 421.31259873 is possible within 100 parts per million (ppm). The **Target frequency** control works in conjunction with the **Set New Frequency** control.

Reset Si570

The **clear** control sets the Si570 programmable oscillator to the default frequency as follows:

Y3 = 644.53125 MHz
Y4 = 706.25 MHz
Y5 = 625 MHz
Y6 = 875 MHz

Set New Frequency

The **Set New Frequency** control sets the Si570 programmable oscillator frequency to the value in the **Target frequency** control. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Altera recommends resetting the FPGA logic after changing frequencies.

Configuring the FPGA Using the Quartus II Programmer

You can use the Quartus II Programmer to configure the FPGA with a specific **.sof**. Before configuring the FPGA, ensure that the Quartus II Programmer and the USB-Blaster driver are installed on the host computer, the USB cable is connected to the transceiver signal integrity development board, power to the board is on, and no other applications that use the JTAG chain are running.

☞ If you connect an external USB-Blaster download cable and power cycle the board, the on-board Blaster is disconnected and the S5_UNLOCK function (Table 4–3 on page 4–4) does not allow JTAG access to the FPGA. To successfully use the USB-Blaster cable, disconnect it before power cycling the board. After you power cycled the board, then reconnect the USB-Blaster cable.

To configure the Stratix V GX FPGA, perform the following steps:

1. Start the Quartus II Programmer.

2. Click **Auto Detect** to display the devices in the JTAG chain.

3. Click **Add File** and select the path to the desired **.sof**.

4. Turn on the **Program/Configure** option for the added file.

5. Click **Start** to download the selected file to the FPGA. Configuration is complete when the progress bar reaches 100%.

☞ Using the Quartus II programmer to configure a device on the board causes other JTAG-based applications such as the Board Test System and the Power Monitor to lose their connection to the board. Restart those applications after configuration is complete.

As you develop your own project using the Altera tools, you can program the flash memory device so that your own design loads from flash memory into the FPGA on power up. This appendix describes the preprogrammed contents of the common flash interface (CFI) flash memory device on the Stratix V GX transceiver signal integrity development board and the Nios II EDS tools involved with reprogramming the user portions of the flash memory device.

The Stratix V GX transceiver signal integrity development board ships with the CFI flash device preprogrammed with a default factory FPGA configuration for running the Board Update Portal design example and a default user configuration for running the Board Test System demonstration. There are several other factory software files written to the CFI flash device to support the Board Update Portal. These software files were created using the Nios II EDS, just as the hardware design was created using the Quartus II software.

For more information about Altera development tools, refer to the Design Software page of the Altera website.

CFI Flash Memory Map

Table A–1 shows the default memory contents of the 1-Gb CFI flash device. For the Board Update Portal to run correctly and update designs in the user memory, this memory map must not be altered.

Table A–1. Byte Address Flash Memory Map

Block Description	Size (KB)	Address Range
Unused	128	0x07FE.0000 - 0x07FF.FFFF
User software	24,320	0x0716.0000 - 0x07FD.FFFF
Factory software	8,192	0x0696.0000 - 0x0715.FFFF
Zipfs (html, web content)	8,192	0x0616.0000 - 0x0695.FFFF
User hardware 2	33,152	0x0410.0000 - 0x0615.FFFF
User hardware 1	33,152	0x020A.0000 - 0x040F.FFFF
Factory hardware	33,152	0x0002.0000 - 0x0209.FFFF
PFL option bits	32	0x0001.8000 - 0x0001.FFFF
Board information	32	0x0001.0000 - 0x0001.7FFF
Ethernet option bits	32	0x0000.8000 - 0x0000.FFFF
User design reset vector	32	0x0000.0000 - 0x0000.7FFF

Altera recommends that you do not overwrite the factory hardware and factory software images unless you are an expert with the Altera tools. If you unintentionally overwrite the factory hardware or factory software image, refer to "Restoring the Flash Device to the Factory Settings" on page A–4.

Preparing Design Files for Flash Programming

You can obtain designs containing prepared **.flash** files from the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page of the Altera website or create **.flash** files from your own custom design.

The Nios II EDS **sof2flash** command line utility converts your Quartus II-compiled **.sof** into the **.flash** format necessary for the flash device. Similarly, the Nios II EDS **elf2flash** command line utility converts your compiled and linked Executable and Linking Format File (**.elf**) software design to **.flash**. After your design files are in the **.flash** format, use the Board Update Portal or the Nios II EDS **nios2-flash-programmer** utility to write the **.flash** files to the user software locations of the flash memory.

For more information about Nios II EDS software tools and practices, refer to the Embedded Software Development page of the Altera website.

Creating Flash Files Using the Nios II EDS

If you have an FPGA design developed using the Quartus II software, and software developed using the Nios II EDS, follow these instructions:

1. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.

2. In the Nios II command shell, navigate to the directory where your design files reside and type the following Nios II EDS commands:

   ■ For Quartus II **.sof** files:

```
sof2flash --input=<yourfile>_hw.sof --output=<yourfile>_hw.flash --offset=0x020A0000
--pfl --optionbit=0x00018000 --programmingmode=PS↵
```

   ■ For Nios II **.elf** files:

```
elf2flash --base=0x0 --end=0x0FFFFFFF --reset=0x07160000 --input=<yourfile>_sw.elf
--output=<yourfile>_sw.flash
--boot=$SOPC_KIT_NIOS2/components/altera_nios2/boot_loader_cfi.srec↵
```

The resulting **.flash** files are ready for flash device programming. If your design uses additional files such as image data or files used by the runtime program, you must first convert the files to **.flash** format and concatenate them into one **.flash** file before using the Board Update Portal to upload them.

☞ The Board Update Portal standard **.flash** format conventionally uses either *<filename>*_**hw.flash** for hardware design files or *<filename>*_**sw.flash** for software design files.

Programming Flash Memory Using the Board Update Portal

Once you have the necessary **.flash** files, you can use the Board Update Portal to reprogram the flash memory. Refer to "Using the Board Update Portal to Update User Designs" on page 5–2 for more information.

☞ If you have generated a **.sof** that operates without a software design file, you can still use the Board Update Portal to upload your design. In this case, leave the **Software File Name** field blank.

Programming Flash Memory Using the Nios II EDS

The Nios II EDS offers a **nios2-flash-programmer** utility to program the flash memory directly. To program the **.flash** files or any compatible S-Record File (**.srec**) to the board using **nios2-flash-programmer**, perform the following steps:

1. Set the Load Selector (J28) to the jump pins 2-3 position to load the Board Update Portal design from flash memory on power up.

2. Attach the USB-Blaster cable and power up the board.

3. If the board has powered up and the LCD displays either "Connecting..." or a valid IP address (such as 152.198.231.75), proceed to step 8. If no output appears on the LCD, or if the D10 for FACTORY_IMAGE LED does not illuminate, continue to step 4 to load the FPGA with a flash-writing design.

4. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–22 for more information.

5. Click **Add File** and select *<install dir>***kits\stratixVGX_5sgxea7nf40_si\factory_recovery\s5gxea7_si_bup.sof**.

6. Turn on the **Program/Configure** option for the added file.

7. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The FACTORY_IMAGE LED (D10) illuminates, indicating that the flash device is ready for programming.

8. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.

9. In the Nios II command shell, navigate to the *<install dir>***kits\stratixVGX_5sgxea7nf40_si\factory_recovery** directory (or to the directory of the **.flash** files you created in "Creating Flash Files Using the Nios II EDS" on page A–2) and type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x0 <yourfile>_hw.flash ↵
```

10. After programming completes, if you have a software file to program, type the following Nios II EDS command:

```
nios2-flash-programmer --base=0x0 <yourfile>_sw.flash ↵
```

11. Set the Load Selector (J28) to the user position (jump pins 1-2) and power cycle the board

Programming the board is now complete.

🕮 For more information about the **nios2-flash-programmer** utility, refer to the *Nios II Flash Programmer User Guide*.

Restoring the Flash Device to the Factory Settings

This section describes how to restore the original factory contents to the flash memory device on the transceiver signal integrity development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch Settings" on page 4–2.

2. Launch the Quartus II Programmer to configure the FPGA with a **.sof** capable of flash programming. Refer to "Configuring the FPGA Using the Quartus II Programmer" on page 6–22 for more information.

3. Click **Add File** and select *<install dir>***kits\stratixVGX_5sgxea7nf40_si\factory_recovery\s5gxea7_si_bup.sof**.

4. Turn on the **Program/Configure** option for the added file.

5. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The FACTORY_IMAGE LED (D10) illuminates, indicating that the flash device is ready for programming.

6. On the Windows Start menu, click **All Programs** > **Altera** > **Nios II EDS** > **Nios II Command Shell**.

7. In the Nios II command shell, navigate to the *<install dir>***kits\stratixVGX_5sgxea7nf40_si\factory_recovery** directory and type the following command to run the restore script:

   ```
   ./restore.sh ↵
   ```

   Restoring the flash memory might take several minutes. Follow any instructions that appear in the Nios II command shell.

8. After all flash programming completes, cycle the POWER switch (SW1) off then on.

9. Using the Quartus II Programmer, click **Add File** and select *<install dir>***kits\stratixVGX_5sgxea7nf40_si\factory_recovery\s5gxea7_si_bup.sof**.

10. Turn on the **Program/Configure** option for the added file.

11. Click **Start** to download the selected configuration file to the FPGA. Configuration is complete when the progress bar reaches 100%. The FACTORY_IMAGE LED (D10) illuminates, indicating that the flash device is ready for programming.

12. Cycle the POWER switch (SW1) off then on to load and run the restored factory design.

13. The restore script cannot restore the board's MAC address automatically. In the Nios II command shell, type the following Nios II EDS command:

    ```
    nios2-terminal ↵
    ```

    and follow the instructions in the terminal window to generate a unique MAC address.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page of the Altera website.

Restoring the MAX II CPLD to the Factory Settings

This section describes how to restore the original factory contents to the MAX II CPLD on the transceiver signal integrity development board. Make sure you have the Nios II EDS installed, and perform the following instructions:

1. Set the board switches to the factory default settings described in "Factory Default Switch Settings" on page 4–2.

    ☞ Setting the switch S7.6 (MAX BYPASS) to open (1) includes the MAX II device in the JTAG chain. Setting the switch S7.6 (MAX BYPASS) to closed (0) removes the Max II device from the JTAG chain.

2. Launch the Quartus II Programmer.

3. Click **Auto Detect**.

4. Click **Add File** and select *<install dir>***kits\stratixVGX_5sgxea7nf40_si\factory_recovery\max2.pof**.

5. Turn on the **Program/Configure** option for the added file.

6. Click **Start** to download the selected configuration file to the MAX II CPLD. Configuration is complete when the progress bar reaches 100%.

To ensure that you have the most up-to-date factory restore files and information about this product, refer to the Transceiver Signal Integrity Development Kit, Stratix V GX Edition page of the Altera website.

This chapter provides additional information about the document and Altera.

Document Revision History

The following table shows the revision history for this document.

Date	Version	Changes
June 2012	1.1	Maintenance release.
September 2011	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact [1]	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1)   You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.

Visual Cue	Meaning
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`.
	Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`.
	Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
☞	The hand points to information that requires special attention.
②	The question mark directs you to a software help system with related information.
👣	The feet direct you to another document or website with related information.
🎦	The multimedia icon directs you to a related multimedia presentation.
⚠ CAUTION	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
⚠ WARNING	A warning calls attention to a condition or possible situation that can cause you injury.
✉	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
💬	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.